Day : Wednesday

Date: 4/11/2007 Time: 12:06:51



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Inventor Name Search Result

Your Search was:

Last Name = TREMBLAY

First Name = MARC

Application#	Patent#	Status	Date Filed	Title	Inventor Name
06338921	Not Issued	161		CLOTHES-DRYER HEAT RECUPERATOR	TREMBLAY, MARC
07381937	Not Issued	164	07/19/1989	CLIP FOR A HANGER	TREMBLAY, MARC
07381938	D315992	150	07/19/1989	CLIP FOR A HANGER	TREMBLAY, MARC
07404203	4984721	250	09/07/1989	GARMENT HANGER	TREMBLAY, MARC
08153814	6128721	150	11/17/1993	TEMPORARY PIPELINE REGISTER FILE FOR A SUPERPIPELINED SUPERSCALAR PROCESSOR	TREMBLAY, MARC
08184044	Not Issued	166	01/21/1994	RAPID REGISTER FILE ACCESS BY LIMITING ACCESS TO A SELECTABLE REGISTER SUB-SET	TREMBLAY, MARC
08363378	Not Issued	166		QUALIFY BIT FOR ANNEX REGISTER FILE	TREMBLAY, MARC
08378659	Not Issued	166		RECONSTRUCTION OF YOUNG BITS IN ANNEX AFTER MISPREDICTED EXECUTION BRANCH IN PIPELINED PROCESSOR	TREMBLAY, MARC
08429651	5611469	150		HANGER WITH IDENTIFICATION CLIP	TREMBLAY, MARC
08603909	5715425	150	02/22/1996	APPARATUS AND METHOD FOR PREFETCHING DATA INTO AN EXTERNAL CACHE	TREMBLAY, MARC
08612623	5778247	150		MULTI-PIPELINE MICROPROCESSOR WITH DATA PRECISION MODE INDICATOR	TREMBLAY, MARC

08641760	Not Issued	168	05/02/1996	METHODS AND APPARATUSES FOR IMPLEMENTING A LOOKUP SWITCH FUNCTION	TREMBLAY, MARC
08642248	Not Issued	168	05/02/1996	METHODS AND APPARATUSES FOR ACCELERATING ARRAY ACCESS BOUNDS CHECKING IN A COMPUTER SYSTEM	TREMBLAY, MARC
08642253	Not Issued	168	05/02/1996	METHODS AND APPARATUSES FOR IMPLEMENTING OPERAND STACK CACHE AS A CIRCULAR BUFFER	TREMBLAY, MARC
08643104	Not Issued	168	05/02/1996	ENHANCED PROCESSOR THAT EXECUTES AN INSTRUCTION SET RECEIVED FROM A PUBLIC CARRIER AND A LOCALLY- RETAINED INSTRUCTION SET	TREMBLAY, MARC
08643984	Not Issued	168	05/07/1996	METHOD AND APPARATUS FOR INSTRUCTION FOLDING FOR A STACK-BASED TYPE PROCESSOR	TREMBLAY, MARC
08643996	Not Issued	168	05/07/1996	APPARATUS AND METHOD FOR ENHANCING OPERATION OF THE JAVA (TM) VIRTUAL MACHINE	TREMBLAY, MARC
08646442	Not Issued	168		APPARATUS AND METHOD FOR ENHANCING THE OPERATIONAL SPEED OF THE JAVA VIRTUAL MACHINE	TREMBLAY, MARC
08647103	Not Issued	168	05/07/1996	METHOD AND APPARATUS FOR STACK HARDWARE PARTITIONING FOR A STACK-BASED TYPE PROCESSOR	TREMBLAY, MARC
08662582	5958042	150	06/11/1996	A GROUPING LOGIC CIRCUIT IN A PIPELINED SUPERSCALAR PROCESSOR	TREMBLAY, MARC
08687293	5721868	150	07/25/1996	RAPID REGISTER FILE ACCESS BY LIMITING ACCESS TO A SELECTABLE REGISTER SUBSET	TREMBLAY, MARC
<u>08752950</u>	5748935	150	11/20/1996	RECONSTRUCTION OF	TREMBLAY,

				YOUNG BITS IN ANNEX AFTER MISPREDICTED EXECUTION BRANCH IN PIPELINED PROCESSOR	MARC
08786351	6026485	150	01/23/1997	INSTRUCTION FOLDING FOR A STACK-BASED MACHINE	TREMBLAY, MARC
08786352	6014723	150	01/23/1997	PROCESSOR WITH ACCELERATED ARRAY ACCESS BOUNDS CHECKING	TREMBLAY, MARC
08786955	6125439	150	01/23/1997	A PROCESS OF EXECUTING A METHOD ON A STACK- BASED PROCESSOR	TREMBLAY, MARC
08787617	6532531	150	01/23/1997	METHOD FRAME STORAGE USING MULTIPLE MEMORY CIRCUITS	TREMBLAY, MARC
08787618	5925123	150	01/23/1997	PROCESSOR FOR EXECUTING INSTRUCTION SETS RECEIVED FROM A NETWORK OR FROM A LOCAL MEMORY	TREMBLAY, MARC
<u>08787736</u>	6038643	150	01/23/1997	A STACK MANAGEMENT UNIT AND METHOD FOR A PROCESSOR HAVING A STACK	TREMBLAY, MARC
08787846	5970242	150	01/23/1997	REPLICATING CODE TO ELIMINATE A LEVEL OF INDIRECTION DURING EXECUTION OF AN OBJECT ORIENTED COMPUTER PROGRAM	TREMBLAY, MARC
08788805	6065108	150	01/23/1997	NON-QUICK INSTRUCTION ACCELERATOR INCLUDING INSTRUCTION IDENTIFIER AND DATA SET STORAGE AND METHOD OF IMPLEMENTING SAME	TREMBLAY, MARC
08788807	6021469	150	01/23/1997	HARDWARE VIRTUAL MACHINE INSTRUCTION PROCESSOR	TREMBLAY, MARC
08788808	5968157	150	01/23/1997	LOCKING OF COMPUTER RESOURCES	TREMBLAY, MARC
08788811	6076141	150	01/23/1997	LOOK-UP SWITCH ACCELERATOR AND METHOD OF OPERATING SAME	TREMBLAY, MARC

08838971	6101580	150	04/23/1997	APPARATUS AND METHOD FOR ASSISTING EXACT GARBAGE COLLECTION BY USING A STACK CACHE OF TAG BITS	TREMBLAY, MARC
08841508	5953736	150	04/23/1997	WRITE BARRIER SYSTEM AND METHOD INCLUDING POINTER-SPECIFIC INSTRUCTION VARIANT REPLACEMENT MECHANISM	TREMBLAY, MARC
08841543	6098089	150	04/23/1997	GENERATION ISOLATION SYSTEM AND METHOD FOR GARBAGE COLLECTION	TREMBLAY, MARC
08841544	5845298	150	04/23/1997	WRITE BARRIER SYSTEM AND METHOD FOR TRAPPING GARBAGE COLLECTION PAGE BOUNDARY CROSSING POINTER STORES	TREMBLAY, MARC
08880253	5875483	150	06/23/1997	COMPLETION UNIT REGISTER FILE USING VIRTUAL ADDRESSES WITH QUALIFY AND PSEUDO- ADDRESS BITS	TREMBLAY, MARC
08880336	6138210	150		MULTI-STACK MEMORY ARCHITECTURE	TREMBLAY, MARC
08880466	6092152	150	06/23/1997	METHOD FOR STACK- CACHING METHOD FRAMES	TREMBLAY, MARC
08880633	6067602	150	06/23/1997	MULTI-STACK-CACHING MEMORY ARCHITECTURE	TREMBLAY, MARC
08880934	6058457	150	06/23/1997	METHOD FOR STORING METHOD FRAMES IN MULTIPLE STACKS	TREMBLAY, MARC
08882796	5873104	150	06/26/1997	BOUNDED-PAUSE TIME GARBAGE COLLECTION SYSTEM AND METHOD INCLUDING WRITE BARRIER ASSOCIATED WITH SOURCE AND TARGET INSTANCES OF A PARTIALLY RELOCATED OBJECT	TREMBLAY, MARC
<u>08882801</u>	5857210	150		BOUNDED-PAUSE TIME GARBAGE COLLECTION SYSTEM AND METHOD INCLUDING READ AND	TREMBLAY, MARC

				WRITE BARRIERS ASSOCIATED WITH AN INSTANCE OF A PARTIALLY RELOCATED OBJECT	
08883291	5873105	150	06/26/1997	BOUNDED-PAUSE TIME GARBAGE COLLECTION SYSTEM AND METHOD INCLUDING WRITE BARRIER ASSOCIATED WITH A SOURCE INSTANCE OF A PARTIALLY RELOCATED OBJECT	TREMBLAY, MARC
08883947	Not Issued	161	06/27/1997		TREMBLAY, MARC
08884580	Not Issued	161			TREMBLAY, MARC
09029022	Not Issued	161	06/12/1998	APPARATUS AND METHOD FOR ADDRESSING CELLS OF INTEREST IN A SOLID STATE SENSOR	TREMBLAY, MARC
09204479	7117342	150	12/03/1998	IMPLICITLY DERIVED REGISTER SPECIFIERS IN A PROCESSOR	TREMBLAY, MARC
09204480	6718457	150	12/03/1998	MULTIPLE-THREAD PROCESSOR FOR THREADED SOFTWARE APPLICATIONS	TREMBLAY, MARC

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Date: 4/11/2007 Time: 12:07:29

Inventor Name Search Result

Your Search was:

Last Name = CHAUDHRY
First Name = SHAILENDER

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09313229	6353881	150	05/17/1999	SUPPORTING SPACE-TIME DIMENSIONAL PROGRAM EXECUTION BY SELECTIVELY VERSIONING MEMORY UPDATES	CHAUDHRY, SHAILENDER
09313243	6247027	150	05/17/1999	FACILITATING GARBAGE COLLECTION DURING OBJECT VERSIONING FOR SPACE AND TIME DIMENSIONAL COMPUTING	CHAUDHRY, SHAILENDER
09327397	6453463	150		METHOD AND APPARATUS FOR PROVIDING FINER MARKING GRANULARITY FOR FIELDS WITHIN OBJECTS	CHAUDHRY, SHAILENDER
09327398	6430649	150	06/07/1999	METHOD AND APPARATUS FOR ENFORCING MEMORY REFERENCE DEPENDENCIES THROUGH A LOAD STORE UNIT	CHAUDHRY, SHAILENDER
09327399	6460067	150		USING TIME STAMPS TO IMPROVE EFFICIENCY IN MARKING FIELDS WITHIN OBJECTS	CHAUDHRY, SHAILENDER
09418625	6658451	150		PARALLEL JOIN OPERATION TO SUPPORT SPACE AND TIME DIMENSIONAL PROGRAM EXECUTION	CHAUDHRY, SHAILENDER
09420335	<u>6463526</u>	150		SUPPORTING MULTI- DIMENSIONAL SPACE-TIME COMPUTING THROUGH OBJECT VERSIONING	CHAUDHRY, SHAILENDER
09422028	<u>6438677</u>	150	l l	DYNAMIC HANDLING OF OBJECT VERSIONS TO	CHAUDHRY, SHAILENDER

				SUPPORT SPACE AND TIME DIMENSIONAL PROGRAM EXECUTION	
09565637	6415356	150	05/04/2000	METHOD AND APPARATUS FOR USING AN ASSIST PROCESSOR TO PRE-FETCH DATA VALUES FOR A PRIMARY PROCESSOR	CHAUDHRY, SHAILENDER
09590935	6714612	150	06/08/2000	METHOD AND DEVICE FOR SYNCHRONIZATION OF PHASE MISMATCH IN COMMUNICATION SYSTEMS EMPLOYING A COMMON CLOCK PERIOD	CHAUDHRY, SHAILENDER
09591142	6704862	150	06/09/2000	METHOD AND APPARATUS FOR FACILITATING EXCEPTION HANDLING USING A CONDITIONAL TRAP INSTRUCTION	CHAUDHRY, SHAILENDER
09592050	6732363	150	06/12/2000	SUPPORTING INTER- PROCESS COMMUNICATION THROUGH A CONDITIONAL TRAP INSTRUCTION	CHAUDHRY, SHAILENDER
09761216	6681318	150	01/16/2001	METHOD AND APPARATUS FOR USING AN ASSIST PROCESSOR TO PREFETCH INSTRUCTIONS FOR A PRIMARY PROCESSOR	CHAUDHRY, SHAILENDER
09761217	7051192	150		FACILITATING VALUE PREDICTION TO SUPPORT SPECULATIVE PROGRAM EXECUTION	CHAUDHRY, SHAILENDER
09761226	6721944	150		MARKING MEMORY ELEMENTS BASED UPON USAGE OF ACCESSED INFORMATION DURING SPECULATIVE EXECUTION	CHAUDHRY, SHAILENDER
09761326	6684398	150	01/16/2001	MONITOR ENTRY AND EXIT FOR A SPECULATIVE THREAD DURING SPACE AND TIME DIMENSIONAL EXECUTION	CHAUDHRY, SHAILENDER
09761360	6772321	150	01/16/2001	METHOD AND APPARATUS FOR USING AN ASSIST PROCESSOR AND VALUE SPECULATION TO FACILITATE PREFETCHING	CHAUDHRY, SHAILENDER

				FOR A PRIMARY PROCESSOR	
10061493	6701417	150	01/31/2002	METHOD AND APPARATUS FOR SUPPORTING MULTIPLE CACHE LINE INVALIDATIONS PER CYCLE	CHAUDHRY, SHAILENDER
10061502	6684297	150	01/31/2002	REVERSE DIRECTORY FOR FACILITATING ACCESSES INVOLVING A LOWER- LEVEL CACHE	CHAUDHRY, SHAILENDER
10061521	6848071	150	01/31/2002	METHOD AND APPARATUS FOR UPDATING AN ERROR- CORRECTING CODE DURING A PARTIAL LINE STORE	CHAUDHRY, SHAILENDER
10061522	6862693	150	01/31/2002	PROVIDING FAULT- TOLERANCE BY COMPARING ADDRESSES AND DATA FROM REDUNDANT PROCESSORS RUNNING IN LOCK-STEP	CHAUDHRY, SHAILENDER
10080859	6934809	150	02/22/2002	AUTOMATIC PREFETCH OF POINTERS	CHAUDHRY, SHAILENDER
10146100	7058877	150	05/14/2002	METHOD AND APPARATUS FOR PROVIDING ERROR CORRECTION WITHIN A REGISTER FILE OF A CPU	CHAUDHRY, SHAILENDER
10146102	7124331	150	05/14/2002	METHOD AND APPARATUS FOR PROVIDING FAULT- TOLERANCE FOR TEMPORARY RESULTS WITHIN A CPU	CHAUDHRY, SHAILENDER
10161794	6754775	150	06/04/2002	METHOD AND APPARATUS FOR FACILITATING FLOW CONTROL DURING ACCESSES TO CACHE MEMORY	CHAUDHRY, SHAILENDER
10184214	6721855	150		USING AN L2 DIRECTORY TO FACILITATE SPECULATIVE LOADS IN A MULTIPROCESSOR SYSTEM	CHAUDHRY, SHAILENDER
10186091	6704841	150	06/26/2002	METHOD AND APPARATUS FOR FACILITATING SPECULATIVE STORES IN A MULTIPROCESSOR SYSTEM	CHAUDHRY, SHAILENDER
10186118	6718839	150	06/26/2002	METHOD AND APPARATUS	CHAUDHRY,

				FOR FACILITATING SPECULATIVE LOADS IN A MULTIPROCESSOR SYSTEM	SHAILENDER
<u>10194856</u>	7152232	150	07/12/2002	HARDWARE MESSAGE BUFFER FOR SUPPORTING INTER-PROCESSOR COMMUNICATION	CHAUDHRY, SHAILENDER
10194911	7168076	150	07/12/2002	FACILITATING EFFICIENT JOIN OPERATIONS BETWEEN A HEAD THREAD AND A SPECULATIVE THREAD	CHAUDHRY, SHAILENDER
10243268	6944724	150	09/13/2002	METHOD AND APPARATUS FOR DECOUPLING TAG AND DATA ACCESSES IN A CACHE MEMORY	CHAUDHRY, SHAILENDER
10288941	7127643	150	11/06/2002	METHOD AND APPARATUS FOR FIXING BIT ERRORS ENCOUNTERED DURING CACHE REFERENCES WITHOUT BLOCKING	CHAUDHRY, SHAILENDER
10365313	Not Issued	161	02/12/2003	Time-multiplexed speculative multi-threading to support single-threaded applications	CHAUDHRY, SHAILENDER
10439911	6862664	150	05/16/2003	METHOD AND APPARATUS FOR AVOIDING LOCKS BY SPECULATIVELY EXECUTING CRITICAL SECTIONS	CHAUDHRY, SHAILENDER
10637165	Not Issued	30	08/08/2003	Commit instruction to support transactional program execution	CHAUDHRY, SHAILENDER
10637166	Not Issued	71	08/08/2003	METHOD FOR REDUCING LOCK MANIPULATION OVERHEAD DURING ACCESS TO CRITICAL CODE SECTIONS	CHAUDHRY, SHAILENDER
10637167	Not Issued	71	08/08/2003	Selectively monitoring stores to support transactional program execution	CHAUDHRY, SHAILENDER
10637168	Not Issued	71	08/08/2003	Selectively monitoring loads to support transactional program execution	CHAUDHRY, SHAILENDER
10637169	Not Issued	41	08/08/2003	Fail instruction to support transactional program execution	CHAUDHRY, SHAILENDER
10686061	7114060	150	10/14/2003	SELECTIVELY DEFERRING INSTRUCTIONS ISSUED IN PROGRAM ORDER	CHAUDHRY, SHAILENDER

				UTILIZING A CHECKPOINT AND MULTIPLE DEFERRAL SCHEME	
10737679	6938130	150	12/15/2003	METHOD AND APPARATUS FOR DELAYING INTERFERING ACCESSES FROM OTHER THREADS DURING TRANSACTIONAL PROGRAM EXECUTION	CHAUDHRY, SHAILENDER
10741944	Not Issued	83	12/19/2003	Generating prefetches by speculatively executing code through hardware scout threading	CHAUDHRY, SHAILENDER
10741949	Not Issued	83	12/19/2003	Performing hardware scout threading in a system that supports simultaneous multithreading	CHAUDHRY, SHAILENDER
10764412	7089374	150	01/23/2004	SELECTIVELY UNMARKING LOAD-MARKED CACHE LINES DURING TRANSACTIONAL PROGRAM EXECUTION	CHAUDHRY, SHAILENDER
10787386	Not Issued	95	02/24/2004	METHOD AND APPARATUS FOR SUPPORTING ONE OR MORE SERVERS ON A SINGLE SEMICONDUCTOR CHIP	CHAUDHRY, SHAILENDER
10895519	7206903	150		METHOD AND APPARATUS FOR RELEASING MEMORY LOCATIONS DURING TRANSACTIONAL EXECUTION	CHAUDHRY, SHAILENDER
10923217	7213133	150	08/20/2004	METHOD AND APPARATUS FOR AVOIDING WRITE- AFTER-WRITE HAZARDS IN AN EXECUTE-AHEAD PROCESSOR	CHAUDHRY, SHAILENDER
10923218	Not Issued	95	08/20/2004	METHOD AND APPARATUS FOR AVOIDING WRITE- AFTER-READ HAZARDS IN AN EXECUTE-AHEAD PROCESSOR	CHAUDHRY, SHAILENDER
10923219	Not Issued	90		METHOD AND APPARATUS FOR AVOIDING READ- AFTER-WRITE HAZARDS IN AN EXECUTE-AHEAD PROCESSOR	CHAUDHRY, SHAILENDER

10932522	Not Issued	30	09/02/2004	Arithmetic early bypass	CHAUDHRY, SHAILENDER		
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Inventor Name Search Result

Your Search was:

Last Name = JACOBSON

First Name = QUINN

Application#	Patent#	Status	Date Filed	Title	Inventor Name	
11126913	Not Issued	41	05/10/2005	Memory latency of processors with configurable stride based pre-fetching technique	JACOBSON, QUINN	
60447128	Not Issued	159	02/13/2003	Transactional memory	JACOBSON, QUINN	
60449956	Not Issued	159	02/25/2003	Method and apparatus for supporting one or more servers on a single semiconductor chip	JACOBSON, QUINN	
60779112	Not Issued	159	03/03/2006	Patchable and/or programmable predecode	JACOBSON, QUINN	
60779113	Not Issued	159	03/03/2006	Patchable and/or programmable decode using predecode selection	JACOBSON, QUINN	
<u>09642075</u>	6757807	150	08/18/2000	EXPLICITLY CLUSTERED REGISTER FILE AND EXECUTION UNIT ARCHITECTURE	JACOBSON, QUINN A.	
09643895	7206925	150	08/18/2000	BACKING REGISTER FILE FOR PROCESSORS	JACOBSON, QUINN A.	
10146100	7058877	150	05/14/2002	METHOD AND APPARATUS FOR PROVIDING ERROR CORRECTION WITHIN A REGISTER FILE OF A CPU	JACOBSON, QUINN A.	
10146102	7124331	150	05/14/2002	I	JACOBSON, QUINN A.	
10349425	Not Issued	41		Method and structure for converting data speculation to control speculation	JACOBSON, QUINN A.	
10439911	<u>6862664</u>	150		l	JACOBSON, QUINN A.	

				SPECULATIVELY EXECUTING CRITICAL	
	<u> </u>		<u></u>	SECTIONS	
10637165	Not Issued	30	08/08/2003	Commit instruction to support transactional program execution	JACOBSON, QUINN A.
10637166	Not Issued	71	08/08/2003	METHOD FOR REDUCING LOCK MANIPULATION OVERHEAD DURING ACCESS TO CRITICAL CODE SECTIONS	JACOBSON, QUINN A.
10637167	Not Issued	71	08/08/2003	Selectively monitoring stores to support transactional program execution	JACOBSON, QUINN A.
10637168	Not Issued	71	08/08/2003	Selectively monitoring loads to support transactional program execution	JACOBSON, QUINN A.
10637169	Not Issued	41		Fail instruction to support transactional program execution	JACOBSON, QUINN A.
10737679	6938130	150	12/15/2003	METHOD AND APPARATUS FOR DELAYING INTERFERING ACCESSES FROM OTHER THREADS DURING TRANSACTIONAL PROGRAM EXECUTION	JACOBSON, QUINN A.
10764412	7089374	.150	01/23/2004	SELECTIVELY UNMARKING LOAD-MARKED CACHE LINES DURING TRANSACTIONAL PROGRAM EXECUTION	JACOBSON, QUINN A.
10787386	Not Issued	95	02/24/2004	METHOD AND APPARATUS FOR SUPPORTING ONE OR MORE SERVERS ON A SINGLE SEMICONDUCTOR CHIP	JACOBSON, QUINN A.
10895519	7206903	150	07/20/2004	METHOD AND APPARATUS FOR RELEASING MEMORY LOCATIONS DURING TRANSACTIONAL EXECUTION	JACOBSON, QUINN A.
10997394	Not Issued	41		Logically partitioning different classes of TLB entries within a single caching structure	JACOBSON, QUINN A.
11026187	Not Issued	30	12/30/2004	Multiple contexts for efficient use	JACOBSON, QUINN A.
11082281	Not Issued	20	03/16/2005	Method and structure for explicit software control of data	JACOBSON, QUINN A.

				speculation	
11082282	Not Issued	41	03/16/2005	Method and structure for explicit software control using scoreboard status information	JACOBSON, QUINN A.
11083163	Not Issued	30	03/16/2005	Method and structure for explicit software control of execution of a thread including a helper subthread	
11093197	Not Issued	41	03/29/2005	Storing results of resolvable branches during speculative execution to predict branches during non-speculative execution	JACOBSON, QUINN A.
11095643	Not Issued	71	03/30/2005	Method and apparatus for facilitating a fast restart after speculative execution	JACOBSON, QUINN A.
11095644	Not Issued	41	03/30/2005	Facilitating rapid progress while speculatively executing code in scout mode	JACOBSON, QUINN A.
11135838	7167970	150	05/23/2005	TRANSLATING LOADS FOR ACCELERATING VIRTUALIZED PARTITION	JACOBSON, QUINN A.
11144097	7191292	150	06/02/2005	LOGGING OF LEVEL-TWO CACHE TRANSACTIONS INTO BANKS OF THE LEVEL- TWO CACHE FOR SYSTEM ROLLBACK	JACOBSON, QUINN A.
11165639	Not Issued	25		Primitives to enhance thread-level speculation	JACOBSON, QUINN A.
<u>11189591</u>	Not Issued	30		Method and apparatus for delaying interfering accesses from other threads during transactional program execution	JACOBSON, QUINN A.
11229247	Not Issued	41	09/16/2005	Centralized BIST engine for testing on-chip memory structures	JACOBSON, QUINN A.
11254286	Not Issued	30	10/19/2005	Technique for thread communication and synchronization	JACOBSON, QUINN A.
<u>11277716</u>	Not Issued	30	:1	PATCHABLE AND/OR PROGRAMMABLE DECODE USING PREDECODE SELECTION	JACOBSON, QUINN A.
11277735	Not Issued	30		PATCHABLE AND/OR PROGRAMMABLE PRE- DECODE	JACOBSON, QUINN A.

I	ı 	1	11.2.12.2.2.2.2		
11296599	Not Issued	40		Start transactional execution (STE) instruction to support transactional program execution	JACOBSON, QUINN A
11322484	Not Issued	30	12/30/2005	Method and apparatus for hardware-based dynamic escape detection in managed run-time environments	JACOBSON, QUINN A.
11349661	Not Issued	30	02/07/2006	Technique for using memory attributes	JACOBSON, QUINN A.
<u>11349787</u>	Not Issued	30	02/07/2006	Hardware acceleration for a software transactional memory system	JACOBSON, QUINN A.
11363625	Not Issued	30	02/28/2006	Return address stack recovery in a speculative execution computing apparatus	JACOBSON, QUINN A.
11394914	Not Issued	30	03/31/2006	Adaptive prefetching	JACOBSON, QUINN A.
11399049	Not Issued	30	04/06/2006	Selectively unmarking load- marked cache lines during transactional program execution	JACOBSON, QUINN A.
11425869	Not Issued	25	06/22/2006	WORKING REGISTER FILE ENTRIES WITH INSTRUCTION BASED LIFETIME	JACOBSON, QUINN A.
11436292	Not Issued	2,5	05/17/2006	Method and system for enhanced thread synchronization and coordination	JACOBSON, QUINN A.
11480090	Not Issued	30	06/30/2006	Concurrent thread execution using user-level asynchronous signaling	JACOBSON, QUINN A.
11534125	Not Issued	25	09/21/2006	EFFECTIVE ELIMINATION OF DELAY SLOT HANDLING FROM A FRONT SECTION OF A PROCESSOR PIPELINE	JACOBSON, QUINN A.
11637661	Not Issued	20	41 1	Protecting memory by containing pointer accesses	JACOBSON, QUINN A.
11646642	Not Issued	19	11	Obscuring memory access patterns	JACOBSON, QUINN A.
60558016	Not Issued	159		Method and apparatus for facilitating a fast restart after speculative execution	JACOBSON, QUINN A.

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